FIG. 1

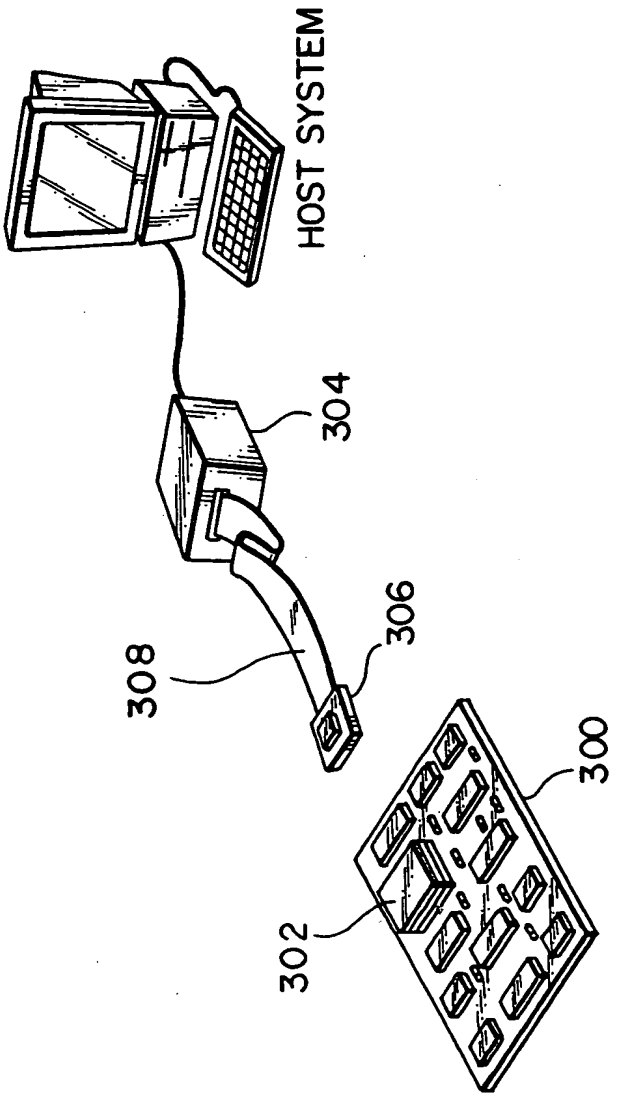

FIG. 2

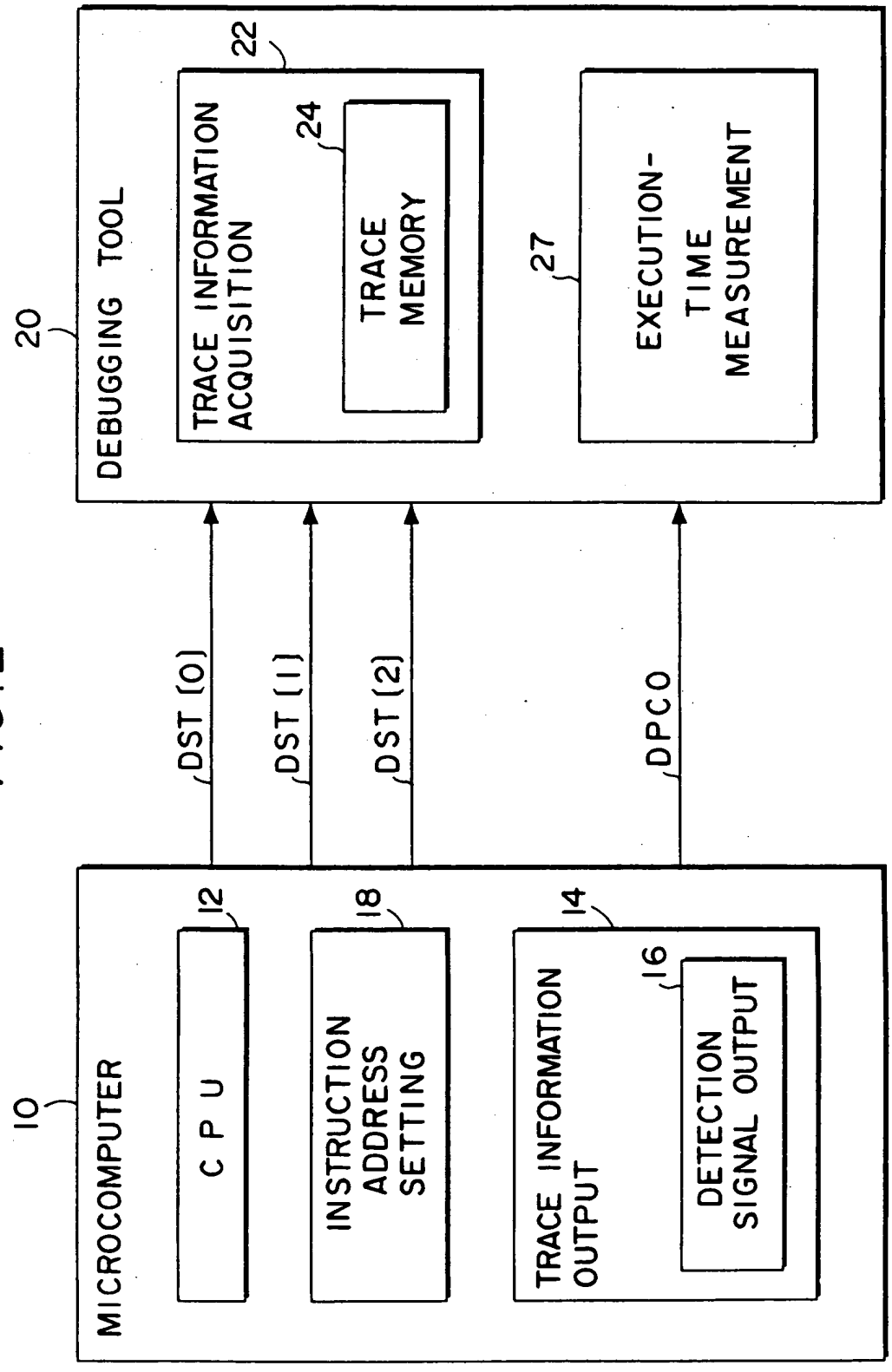
10
MICROCOMPUTER
12
C P U
18
INSTRUCTION ADDRESS SETTING
14
TRACE INFORMATION OUTPUT
16
DETECTION SIGNAL OUTPUT
DST (0)
DST (1)
DST (2)
DPC0
20
DEBUGGING TOOL
22
TRACE INFORMATION ACQUISITION
24
TRACE MEMORY
27
EXECUTION-TIME MEASUREMENT

FIG. 3

	DST (2)	DST (1)	DST (0)	CPU INSTRUCTION EXECUTION STATE
	0	0	0	ORDINARY INSTRUCTION EXECUTION END (EXECUTION END IN ADDRESS SEQUENCE)
	0	0	1	PC RELATIVE BRANCH INSTRUCTION EXECUTION
	0	1	0	PC ABSOLUTE BRANCH INSTRUCTION EXECUTION
	0	1	1	IDLE CYCLE
310	1	0	0	MATCH WITH INSTRUCTION BREAK DURING ORDINARY INSTRUCTION EXECUTION
310	1	0	1	MATCH WITH INSTRUCTION BREAK DURING PC RELATIVE BRANCH INSTRUCTION EXECUTION
310	1	1	0	MATCH WITH INSTRUCTION BREAK DURING PC ABSOLUTE BRANCH INSTRUCTION EXECUTION
312	1	1	1	BREAK SPACE (DEBUGGING MODE)

FIG. 4A

OUTPUT DURING ORDINARY OPERATION

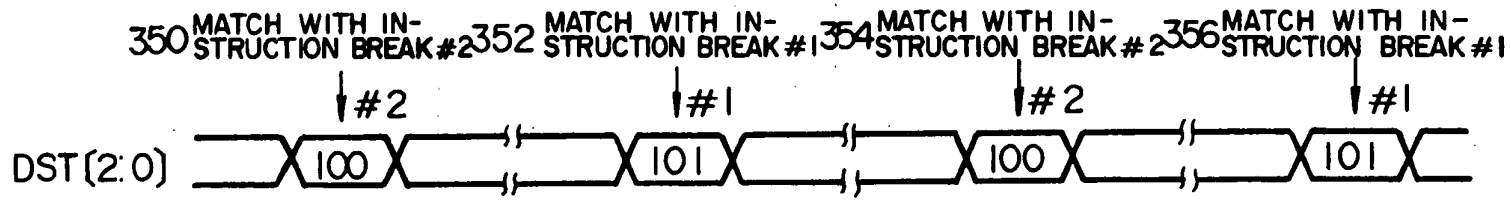

FIG. 4B

OUTPUT DURING REPEATED MATCHES WITH INSTRUCTION BREAKS

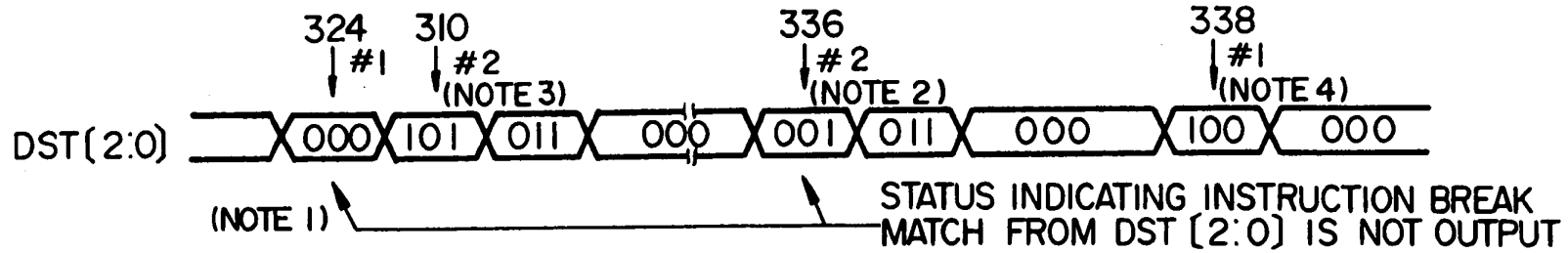

FIG. 4C

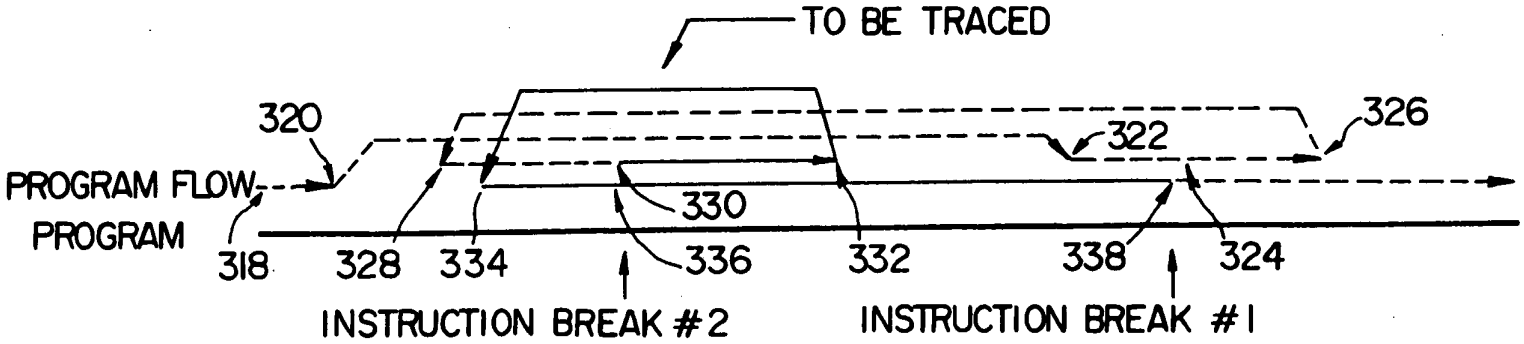

FIG. 5


370 TRACE RANGE 1
372 TRACE RANGE 2
DST[2]
1
2
3
4
BREAK #2
360
BREAK #1
362
BREAK #2
364
BREAK #1
366

FIG. 6

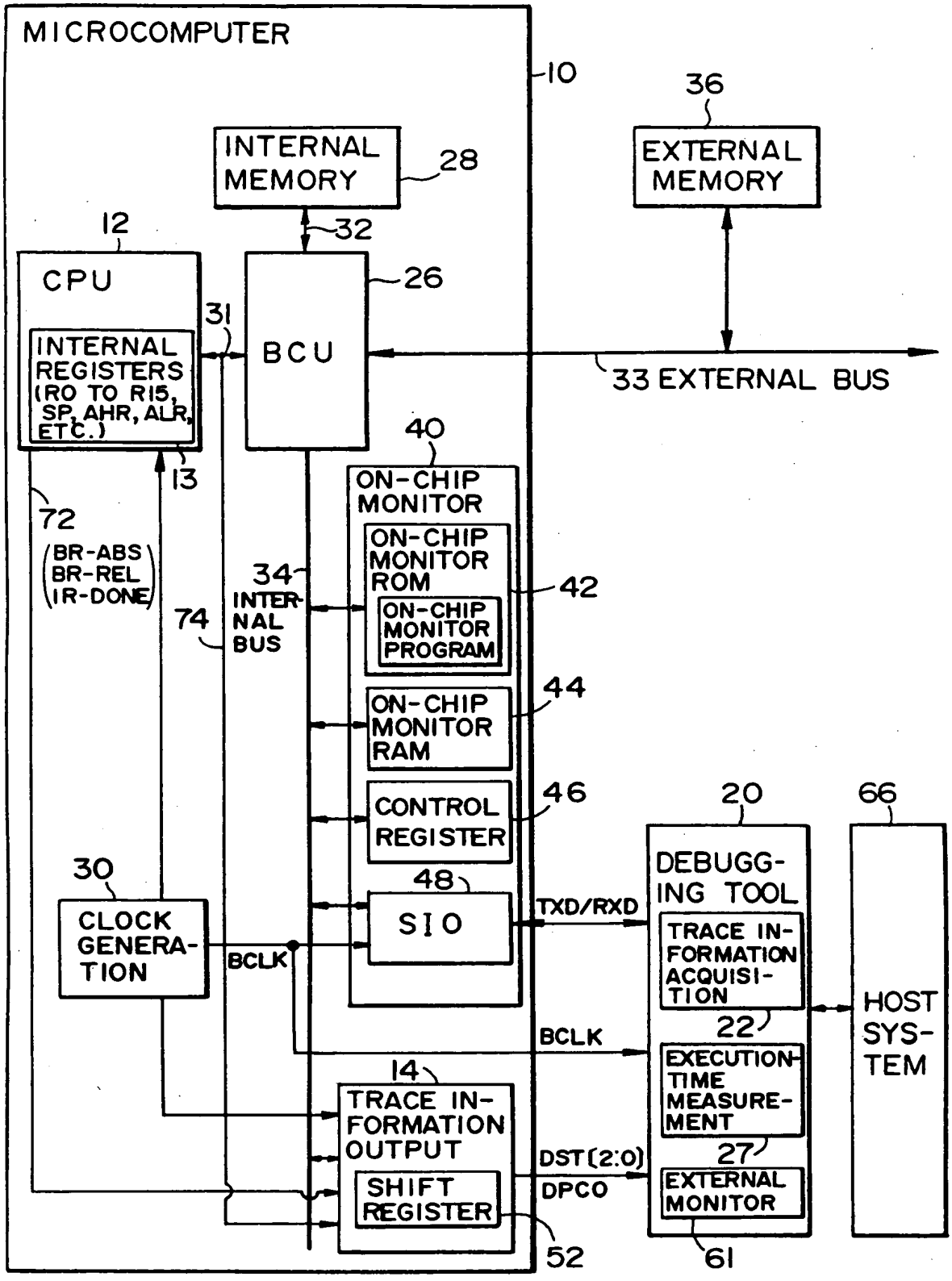
MICROCOMPUTER
10
36
INTERNAL MEMORY
28
EXTERNAL MEMORY
12
32
CPU
26
31
INTERNAL REGISTERS (R0 TO R15, SP, AHR, ALR, ETC.)
BCU
33 EXTERNAL BUS
40
ON-CHIP MONITOR
13
72
(BR-ABS BR-REL IR-DONE)
34
INTERNAL BUS
74
ON-CHIP MONITOR ROM
42
ON-CHIP MONITOR PROGRAM
44
ON-CHIP MONITOR RAM
46
CONTROL REGISTER
20
66
30
48
CLOCK GENERATION
SIO
TXD/RXD
DEBUGGING TOOL
TRACE INFORMATION ACQUISITION
BCLK
BCLK
22
HOST SYSTEM
14
EXECUTION-TIME MEASUREMENT
TRACE INFORMATION OUTPUT
DST(2:0)
27
DPCO
SHIFT REGISTER
EXTERNAL MONITOR
52
61

FIG. 7

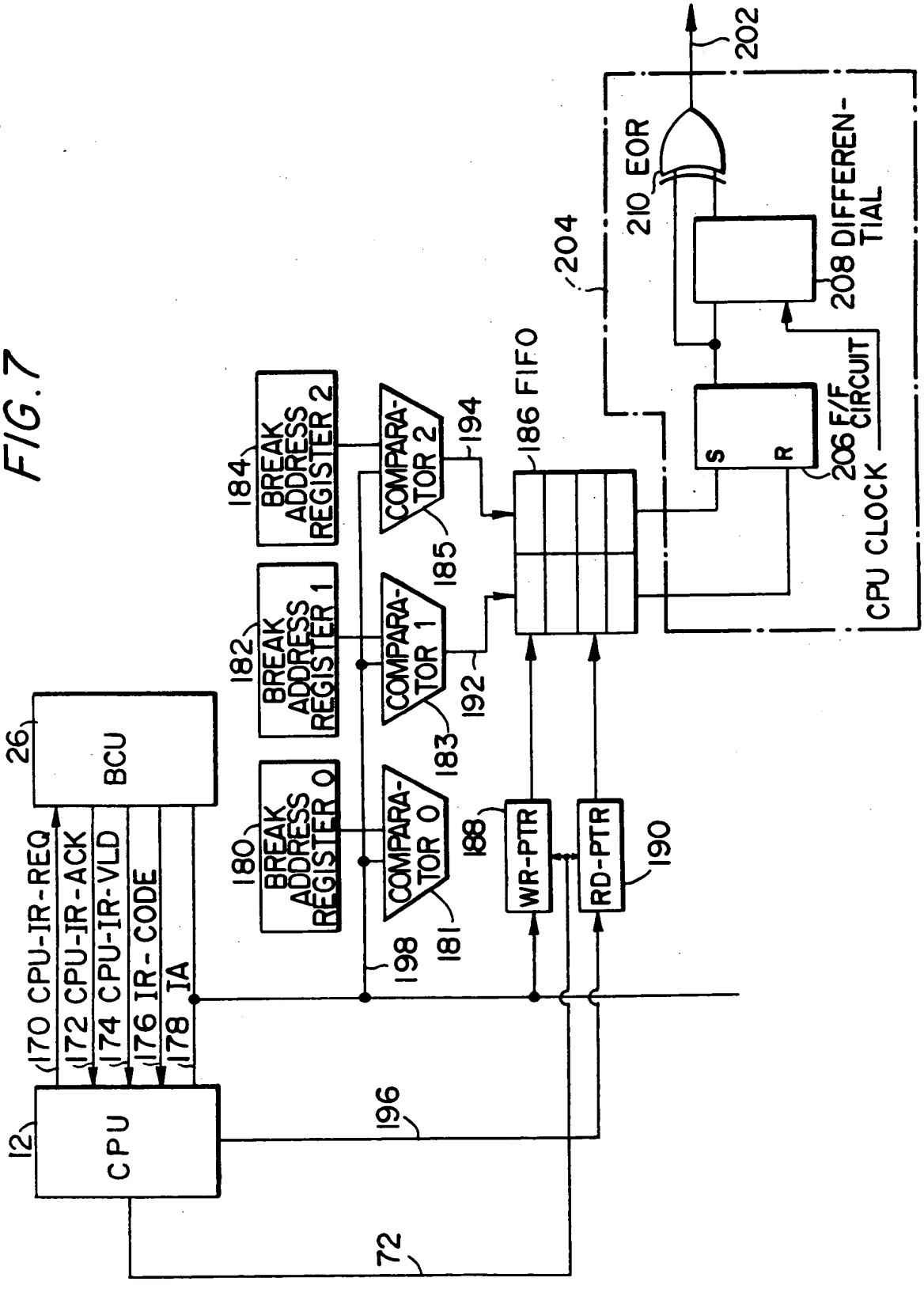
12
CPU
26
BCU
170 CPU-IR-REQ
172 CPU-IR-ACK
174 CPU-IR-VLD
176 IR-CODE
178 IA
72
196
180
BREAK ADDRESS REGISTER 0
182
BREAK ADDRESS REGISTER 1
184
BREAK ADDRESS REGISTER 2
181
COMPARA-TOR 0
183
COMPARA-TOR 1
185
COMPARA-TOR 2
188
WR-PTR
190
RD-PTR
186 FIFO
192
194
198
204
210 EOR
202
208 DIFFEREN-TIAL
206 F/F CIRCUIT
S
R
CPU CLOCK

FIG. 8

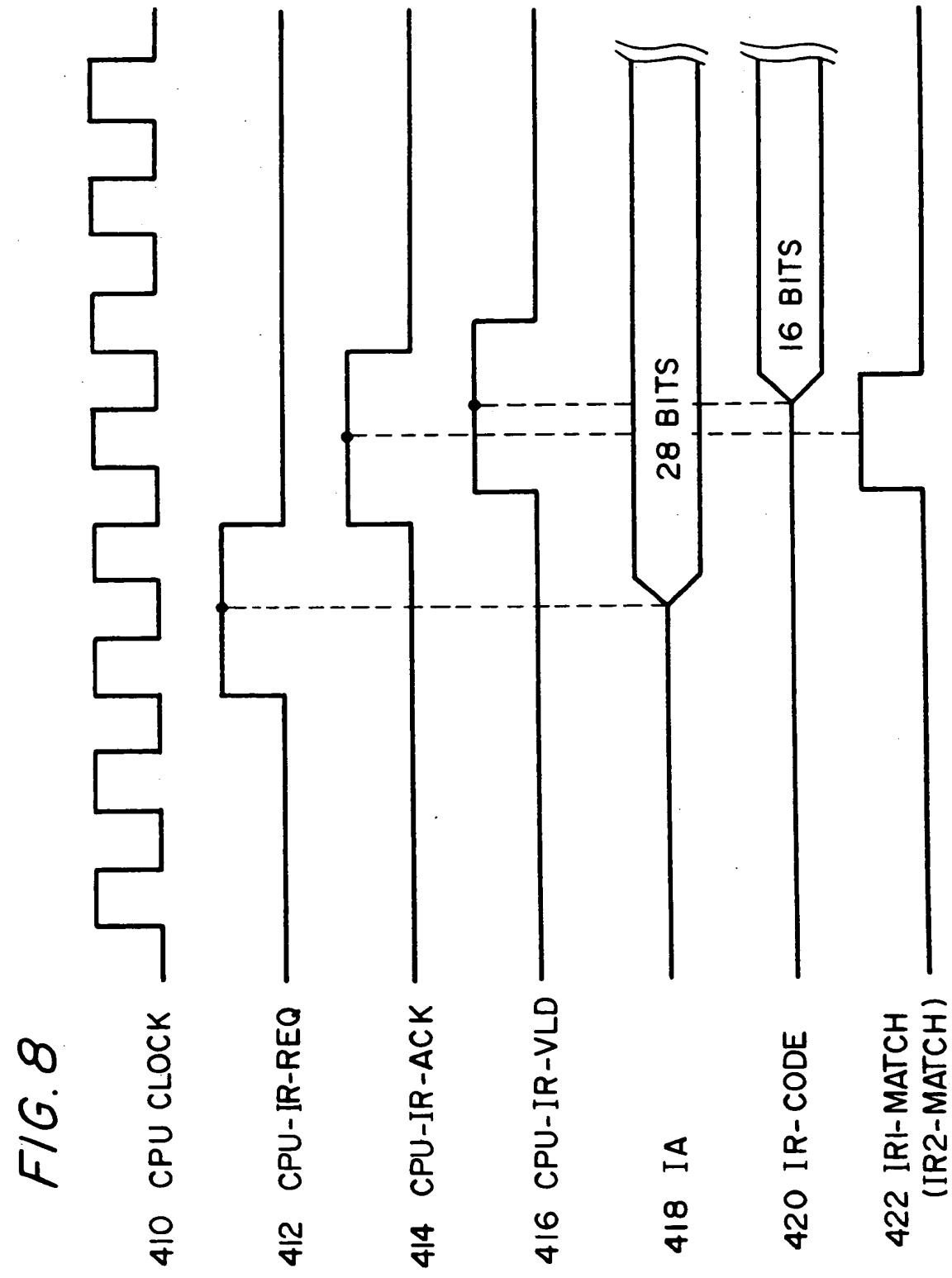
410 CPU CLOCK
412 CPU-IR-REQ
414 CPU-IR-ACK
416 CPU-IR-VLD
418 IA
28 BITS
420 IR-CODE
16 BITS
422 IRI-MATCH
(IR2-MATCH)

FIG. 9A

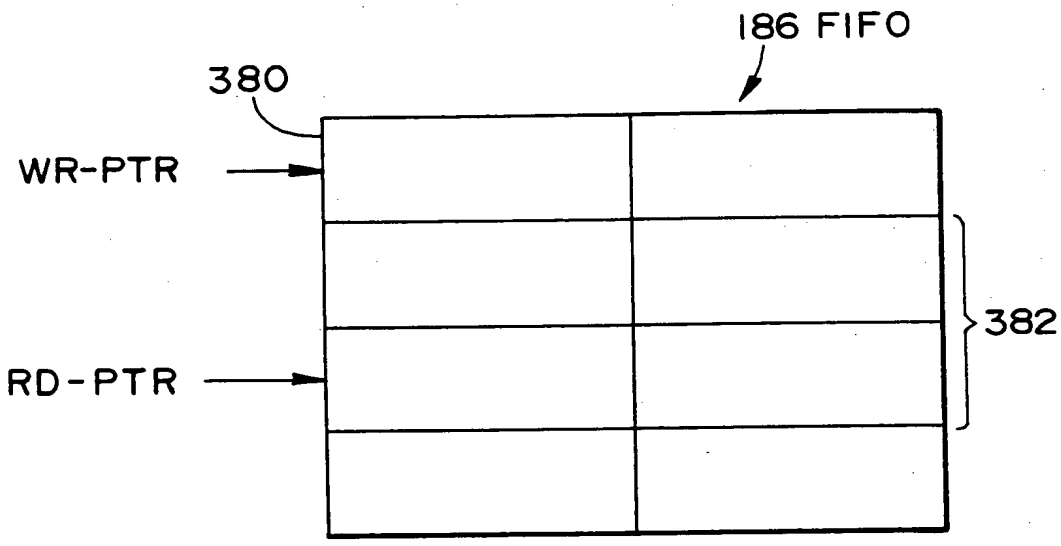

FIG. 9B

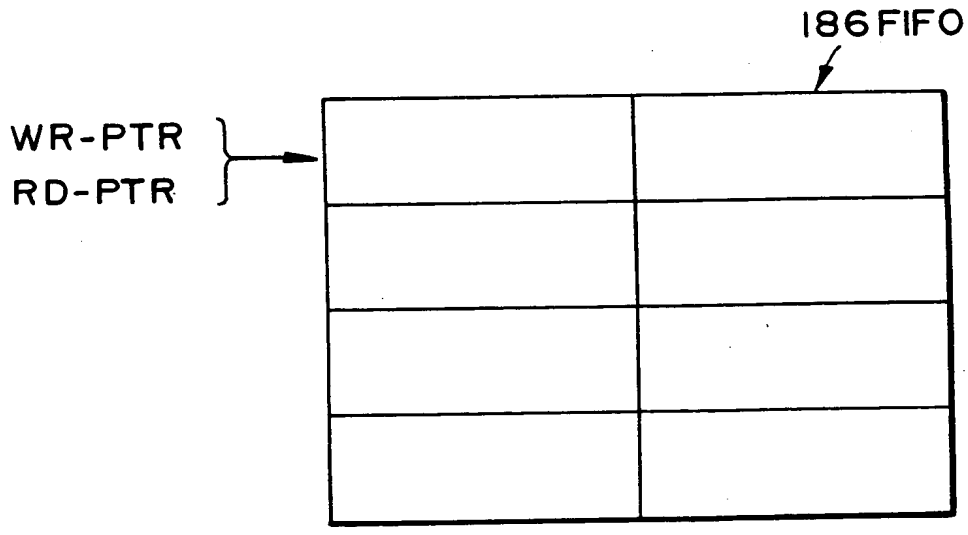

FIG.10

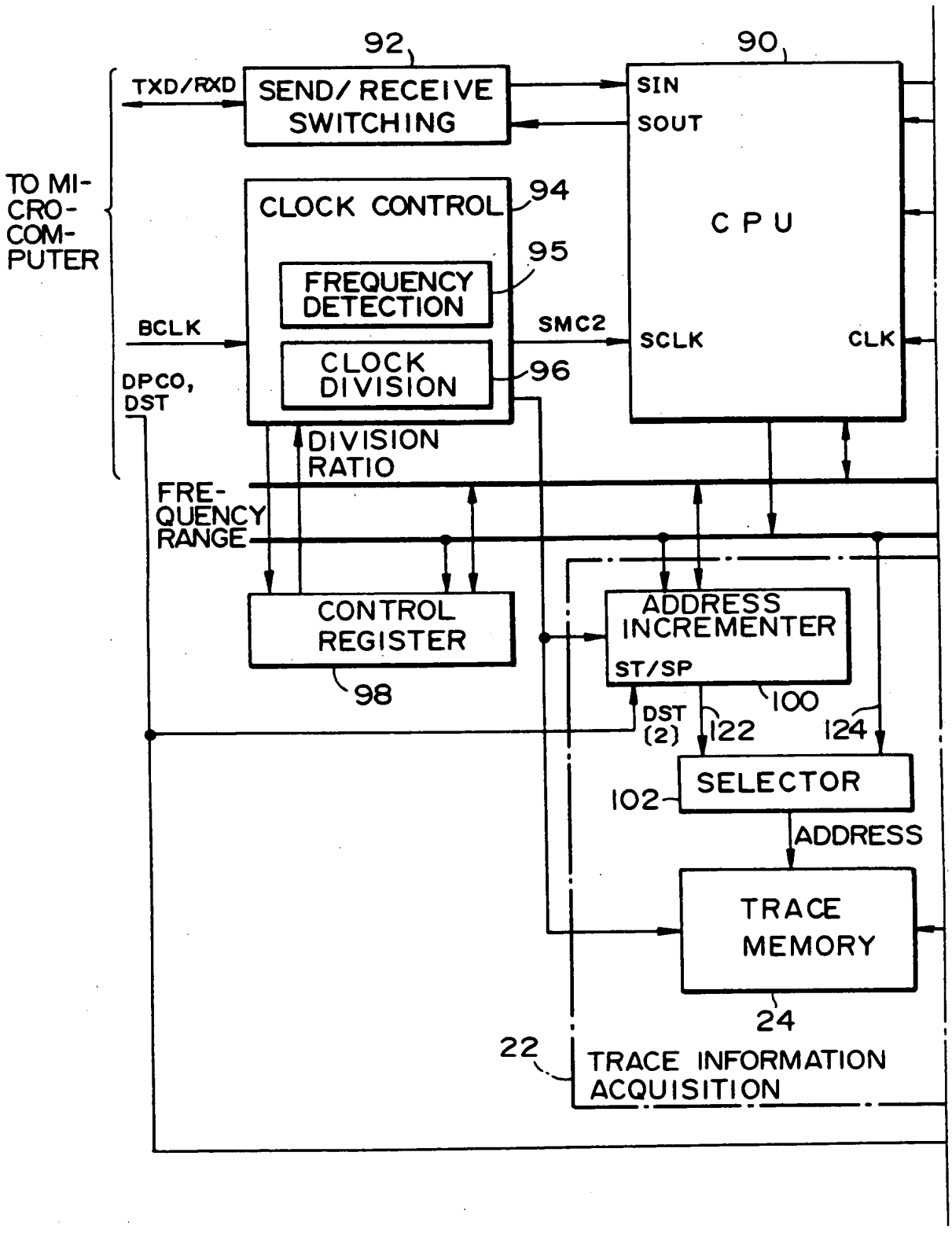
92
90
TXD/RXD
SEND/ RECEIVE SWITCHING
SIN
SOUT
TO MI-CRO-COM-PUTER
CLOCK CONTROL
94
C P U
95
FREQUENCY DETECTION
BCLK
SMC2
SCLK
CLK
CLOCK DIVISION
96
DPCO, DST
DIVISION RATIO
FRE-QUENCY RANGE
CONTROL REGISTER
98
ADDRESS INCREMENTER
ST/SP
100
DST (2)
122
124
SELECTOR
102
ADDRESS
TRACE MEMORY
24
22
TRACE INFORMATION ACQUISITION

FIG.10 (con't)

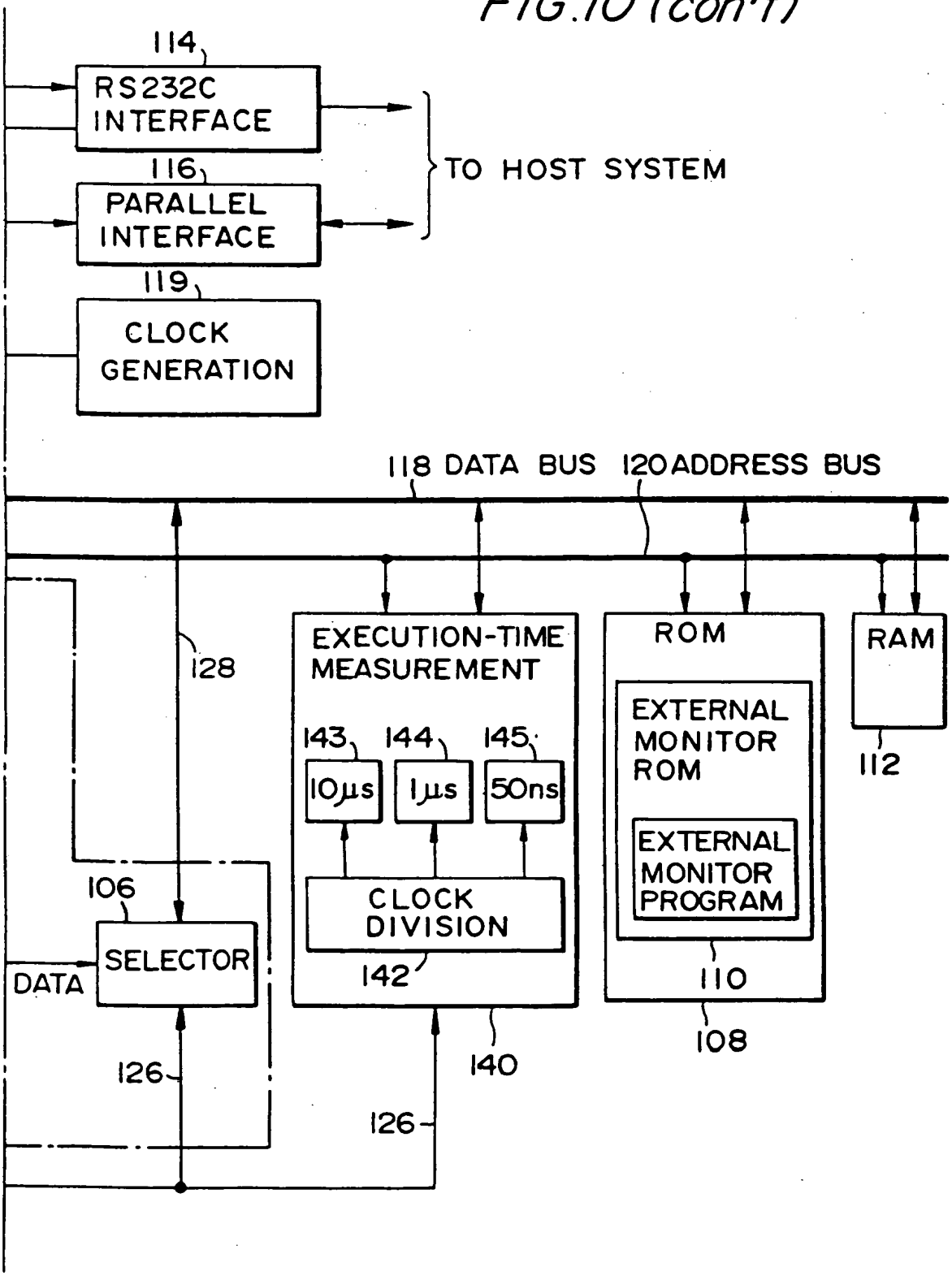
114
RS232C INTERFACE
116
PARALLEL INTERFACE
TO HOST SYSTEM
119
CLOCK GENERATION
118 DATA BUS
120 ADDRESS BUS
128
EXECUTION-TIME MEASUREMENT
143
144
145
10μs
1μs
50ns
CLOCK DIVISION
142
ROM
EXTERNAL MONITOR ROM
EXTERNAL MONITOR PROGRAM
110
108
RAM
112
106
SELECTOR
DATA
126
126
140

FIG.11A

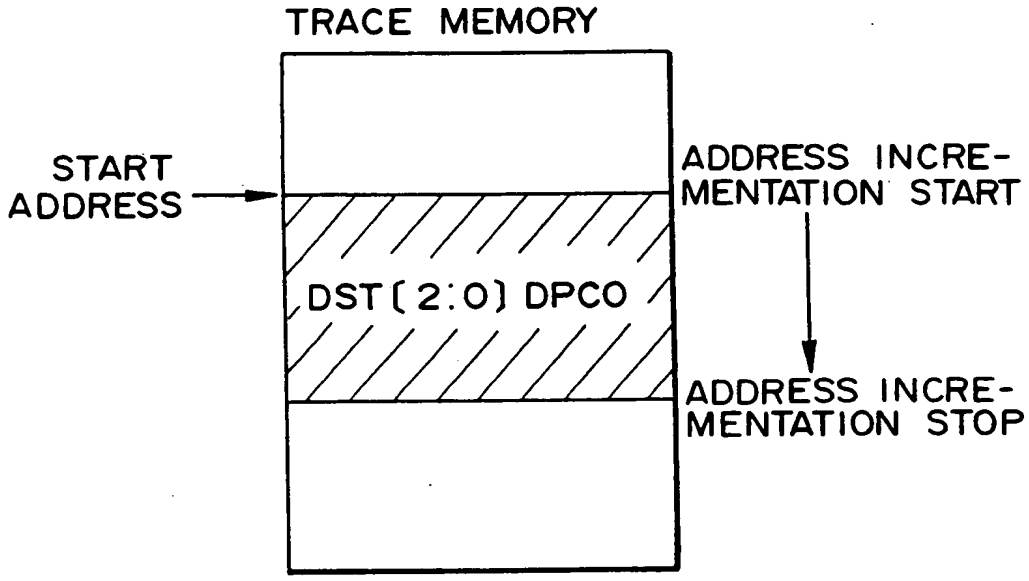

FIG.11B

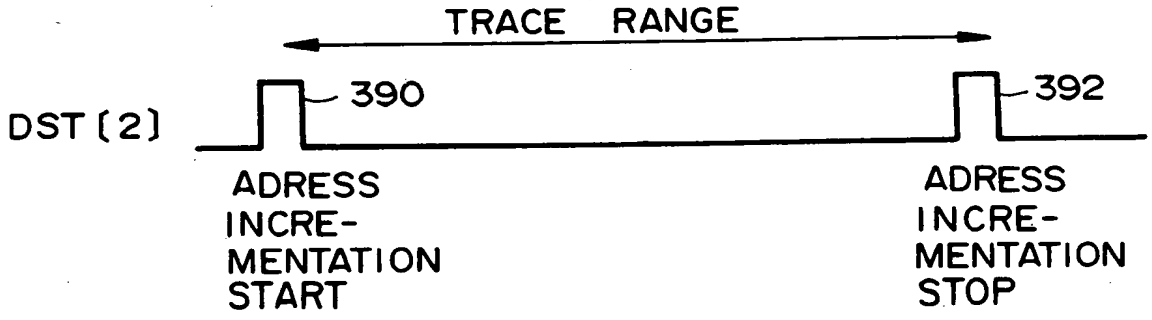

FIG. 12A

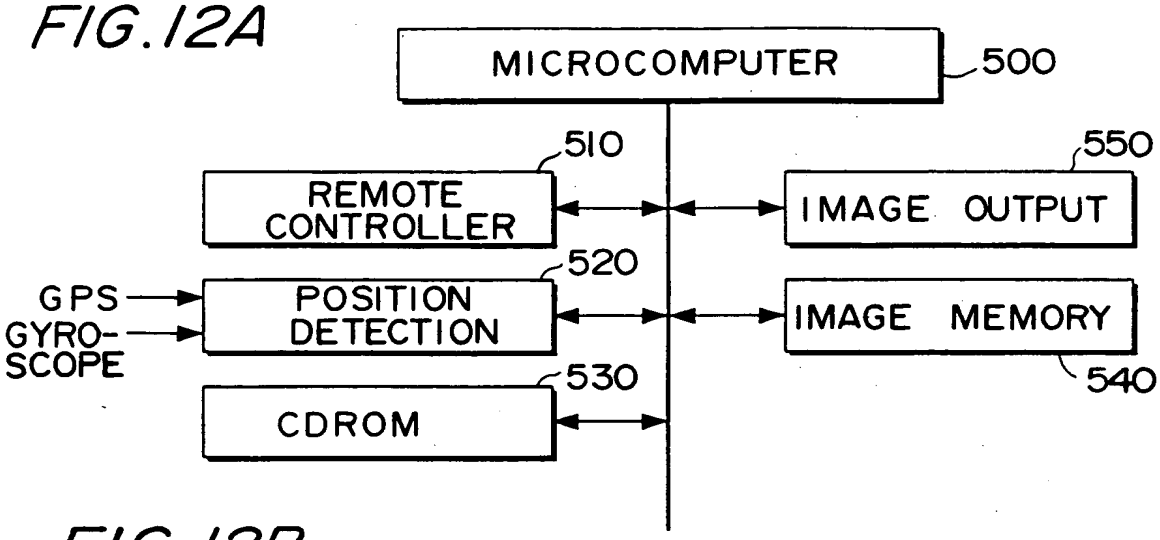

FIG. 12B

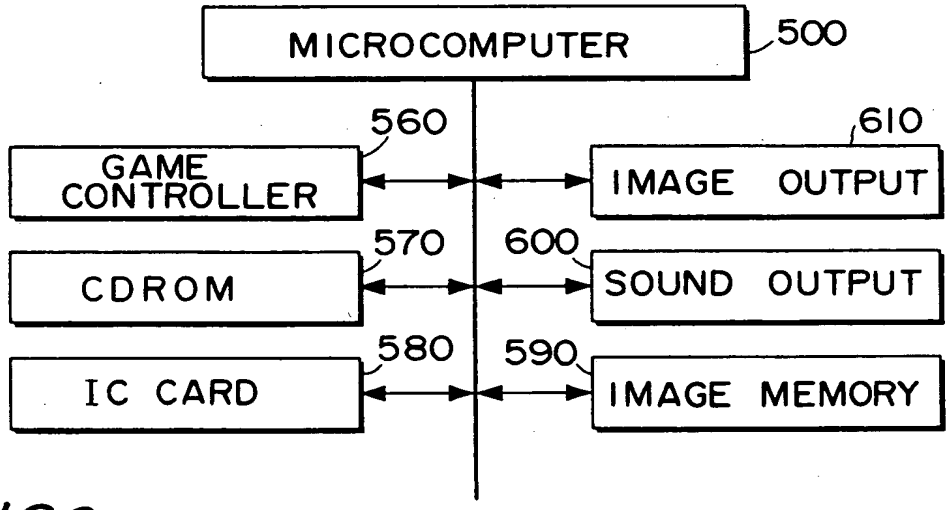

FIG. 12C

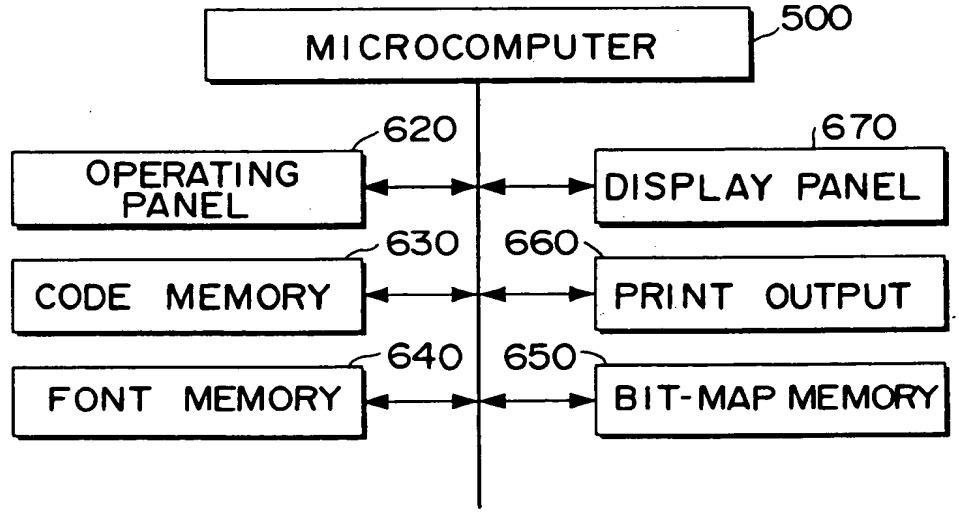

FIG. 13A

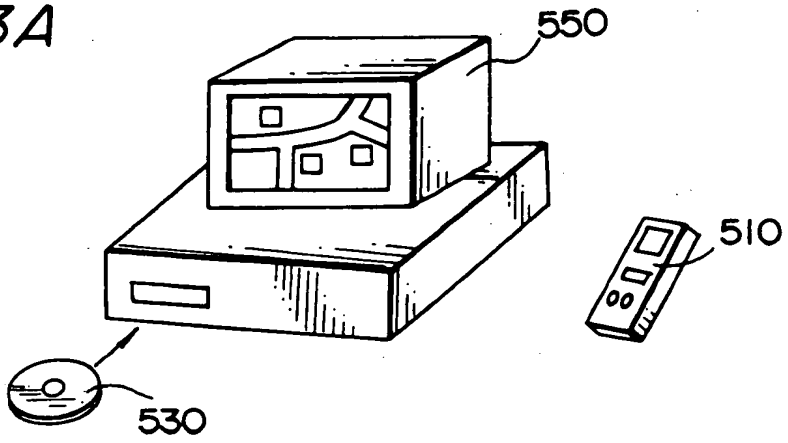

FIG. 13B

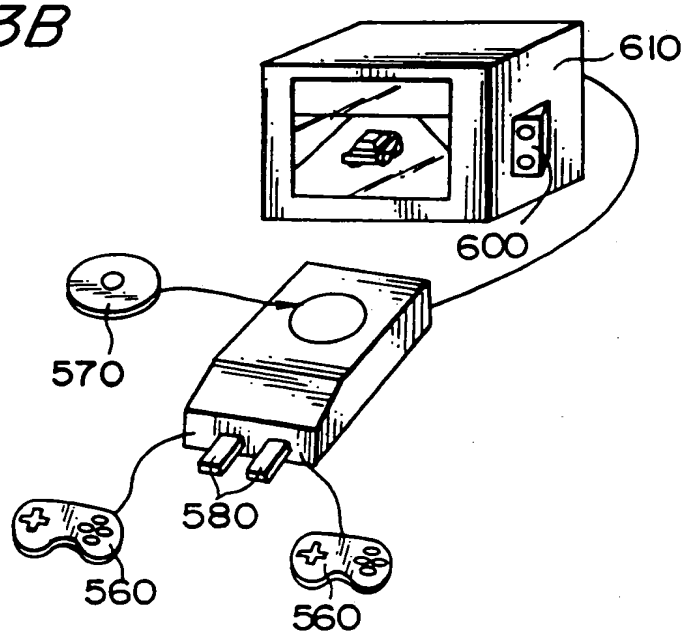

FIG. 13C